Effect of sidewall surface recombination on the quantum efficiency in a Y_2O_3 passivated gated type-II InAs/GaSb long-infrared photodetector array

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Y_2O_3 was applied to passivate a long-wavelength infrared type-II superlattice gated photodetector array with 50% cut-off wavelength at 11 μm, resulting in a saturated gate bias that was 3 times lower than in a SiO_2 passivated array. Besides effectively suppressing surface leakage, gating technique exhibited its ability to enhance the quantum efficiency of $100 \times 100\,\mu$m size mesa from 51% to 57% by suppressing sidewall surface recombination. At 77 K, the gated photodetector showed dark current density and resistance-area product at -300 mV of 2.5×10^{-5} A/cm^2 and $1.3 \times 10^4\,\Omega\,$cm^2, respectively, and a specific detectivity of 1.4×10^{12} Jones. © *2013 AIP Publishing LLC*. [http://dx.doi.org/10.1063/1.4833026]

Type-II InAs/GaSb superlattice (T2SL) has shown its great capability for infrared detection and imaging.[1] Although many aspects of these detectors are rapidly being improved,[2–9] the performance of T2SL has not yet reached its theoretical capacities.[10] Partly this is due to the surface leakage current, which is particularly severe in the long-wavelength infrared region (LWIR). Surface leakage current originates from the abrupt termination of the periodic crystalline structure on the mesa sidewall after etching, which creates dangling bonds on the mesa sidewall. These dangling bonds can be easily occupied by byproducts from processing and interfacial fixed charges from the passivation layer, resulting in electron accumulation and type inversion at sidewall surfaces.[11,12] The effect of surface leakage current is more pronounced in the small size pixels and becomes a limiting factor for scaling down focal plane array (FPA) pixel size for higher resolution. Therefore, different approaches were attempted to suppress the surface leakage current, including double heterostructure design,[13] graded doping combined with shallow etch,[14] inductively coupled plasma (ICP) dry etch,[15] regrowth of wide band gap material,[16] and different passivation techniques.[17–22] However, the surface leakage problem has not been solved, and the performance of T2SL photodetector is still limited by surface leakage current.

Recently, the gating technique, involving a metal-insulator-semiconductor (MIS) structure on the mesa sidewall that actively controls the surface potential, has shown its great ability to eliminate the surface leakage current in both mid-wavelength infrared (MWIR) and LWIR T2SL P^+-π-M-N^+ photodetectors, improve detectivity, widen the detector's operation range, and provide deeper understanding of the surface leakage phenomenon.[11,12] At large negative gate bias ($V_G = -40$ V), the surface leakage current is eliminated in the SiO_2 passivated MWIR T2SL P^+-π-M-N^+ photodetector.[11] The high saturated gate bias (later noted as $V_{G,sat}$) can be suppressed by reducing the dielectric layer thickness.[12] However, once the SiO_2 layer thickness is reduced to 7–10 nm range, the dielectric may suffer from relatively low breakdown voltage and high gate leakage current because of high pinhole densities and enhanced tunneling current.[23] Moreover, a high quality dielectric layer with certain minimum thickness is required for protecting the mesa during the chemically and mechanically aggressive FPA fabrication steps that follow the passivation. As a result of this incompatibility between the processing and operating requirements, gated T2SL photodetectors have not yet been realized at the FPA level. In order to achieve low $V_{G,sat}$ value, without making compromise on dielectric thickness, SiO_2 must be replaced with high-k dielectric material. Yttrium sesquioxide (Y_2O_3) has been considered as gate oxide material to replace SiO_2 in the metal-oxide-semiconductor (MOS) devices because of its wide band gap (Eg = 5.6 eV), high thermal and chemical stability, mechanical robustness, a relatively high dielectric constant (k = 12–18), and high breakdown field strength.[23–28] At the same time, since the gated diodes (GD) are covered by a passivation layer, the quantum efficiency (QE) and the specific detectivity (D*) of those kinds of diodes cannot be measured directly in the front-side illumination configuration without knowing the transmission spectrum of the passivation layer. Most importantly, the influence of surface leakage on the QE of T2SL photodetector has not been investigated yet, and the gated photodetector with back-side illumination configuration is needed for having a deeper understanding of surface leakage phenomena. In this letter we take the advantage of a gated photodetector array to report the influence of the surface recombination on the QE of LWIR T2SL P^+-π-M-N^+ photodetector measured with back-side illumination.

The LWIR material in this work was grown on an n-type GaSb substrate with a Gen-II Molecular Beam Epitaxy (MBE) reactor. After 0.1 μm thick GaSb buffer layer, a 1.5 μm thick n-doped InAsSb etch stop layer was grown, followed by a 5.5 μm thick N^+-M-π-P^+ superlattice device, and finished with 20 nm thick P^+-doped InAs capping layer. The thickness of N^+-contact ($n^+ \sim 10^{18}$ cm^{-3}) and lightly n-doped M-barrier[6] were both 0.5 μm, and their superlattice periods consisted of 18/3/5/3 monolayers (MLs) of InAs/GaSb/AlSb/GaSb in one period. The N^+-region and M-barrier were both doped with silicon. The 4 μm thick lightly p-doped π-region ($p^- \sim 10^{16}$ cm^{-3}) contained 13/7

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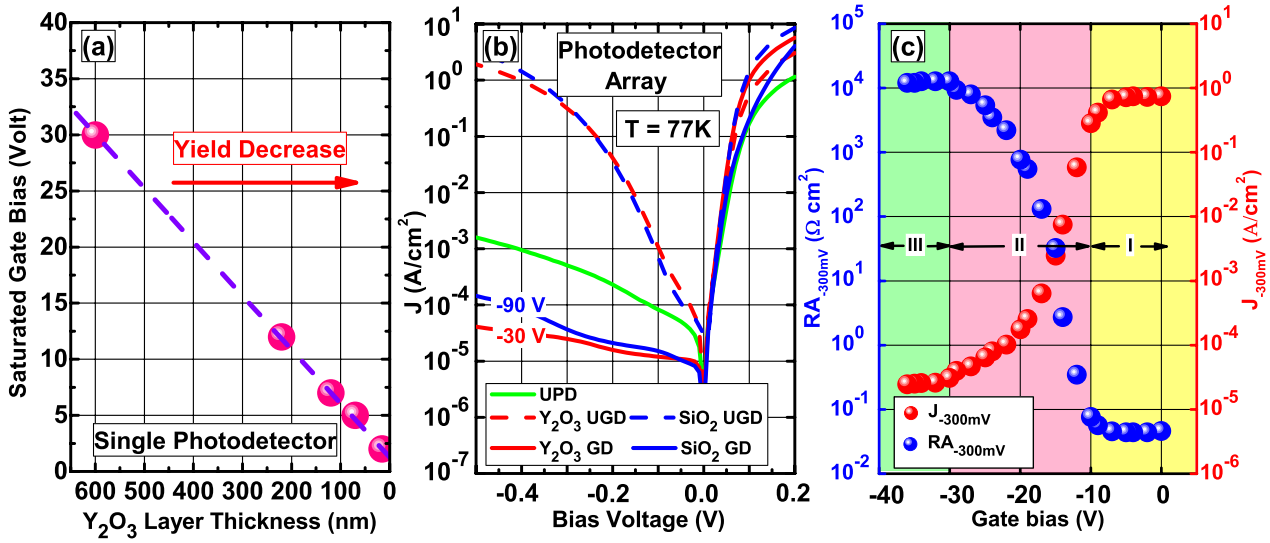

FIG. 1. (a) Correlation between saturated gate bias and Y_2O_3 passivation layer thickness of samples A2–A6. (b) Comparison of dark current density of the UPD and UGD with SiO_2 and Y_2O_3 passivation, and GD with SiO_2 and Y_2O_3 passivation. (c) The dependence of reverse dark current density and differential resistance area product on gate bias in Y_2O_3 passivated GDs at $V_{op} = -300$ mV.

MLs of InAs/GaSb, and the 0.5 μm thick P^+-contact region ($p^+ \sim 10^{18}$ cm^{-3}) was composed of 7/11 MLs of InAs/GaSb. The π-region and P^+-contact were doped with beryllium.

The material was processed into eight dies of photodetectors by applying standard contact lithography. Samples A1–A6 contain single gated photodetectors, which have individual gate contacts to each photodetector, and samples B and C contain photodetector arrays, which each have one common gate contact for the whole array. Samples A1–A6 contain circular and square diodes ranging from 100 to 400 μm in diameter or on a side while samples B and C contain square detector arrays with pixel size of 100×100 μm. Pixels were delineated by electron cyclotron resonance-reactive ion etching (ECR-RIE) and citric-acid based wet etching, followed by top and bottom metal contacts deposition by electron beam metal evaporation. Sample A1 was kept unpassivated, and those unpassivated diodes (UPD) were used for reference. Sample B was passivated with 600 nm thick SiO_2 using plasma-enhanced chemical vapor deposition (PECVD), and samples A2–A6 and C were passivated with Y_2O_3 using ion-beam sputtering deposition (IBD). The Y_2O_3 passivation layer thicknesses of A2–A6 were 15 nm, 70 nm, 120 nm, 220 nm, and 600 nm. Although the $V_{G,sat}$ of sample A2 was as low as -2 V (Figure 1(a)), 600 nm thick Y_2O_3 passivation layers were used for array fabrication (sample C) to prevent leakage at the common gate contact. Half of the single photodetectors on samples A2–A6 and the half of the array on samples B and C had a gate metal contact deposited on their mesa sidewalls so that sample B and C contained both GD arrays and ungated diode (UGD) arrays. The regions of dielectric layer covering the top and bottom contacts were etched away by using CF_4:Ar^+ plasma for SiO_2 and Ar^+ plasma for Y_2O_3 in a ECR-RIE system. After that, the processing of samples A2–A6 was finished. Indium bumps were then deposited in a thermal evaporator for sample B and C, and then both were flip-chip bonded to a silicon fan-out, underfilled, and their substrates were removed up to the InAsSb etch stop layer. No antireflective coating was applied to any sample. Table I gives the summary about type and thickness of passivation layer, $V_{G,sat}$, and type of diode on each sample.

Average I-V characteristics of UPDs, UGDs, and GDs at $V_G = V_{G,sat}$ are compared in Figure 1(b). The diode operation bias (V_{op}) of this sample is -300 mV because of bias dependent optical behavior (inset of Figure 2). Both SiO_2 and Y_2O_3 passivated UGDs suffer much leakier I-V characteristics than the UPDs because the fixed charges in the SiO_2/T2SL and Y_2O_3/T2SL interfaces cause type-inversion on the mesa sidewall surface and result in high surface tunneling leakage current.[12] From the close match between SiO_2 and Y_2O_3 passivated UGD's IV curves, one can infer that the Y_2O_3/T2SL and SiO_2/T2SL interfaces have similar interface charge densities. The actual interfaces charge densities can be compared according to the following formula:

$$\sigma_{Y_2O_3} = \left(\varepsilon_{Y_2O_3} V_{G,sat}^{Y_2O_3} \sigma_{SiO_2} d_{SiO_2}\right) \Big/ \left(\varepsilon_{SiO_2} V_{G,sat}^{SiO_2} d_{Y_2O_3}\right), \quad (1)$$

TABLE I. Type of passivation, passivation layer thickness, saturated gated bias, and available types of diode on each sample.

Sample	A1	A2	A3	A4	A5	A6	B	C
Sample type				Single photodetector			Array	
Passivation	No	Y_2O_3	Y_2O_3	Y_2O_3	Y_2O_3	Y_2O_3	SiO_2	Y_2O_3
Passivation thickness (nm)	No	15 nm	70 nm	120 nm	220 nm	600 nm	600 nm	600 nm
$V_{G,sat}$ (V)	No	-2	-5.5	-7	-12	-30	-90	-30
Diode type	UPD			UGD/GD			UGD/GD	

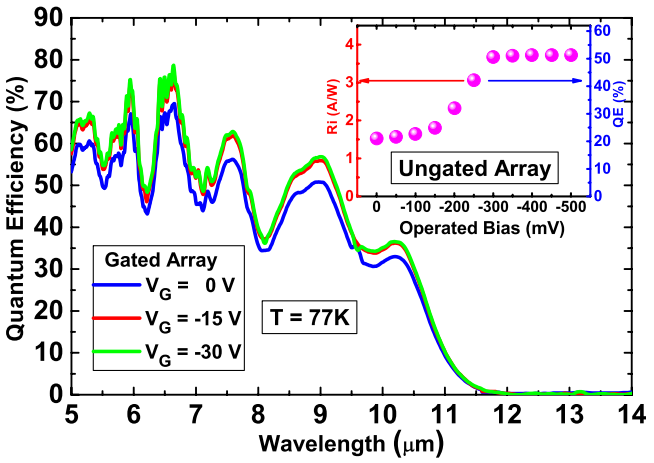

FIG. 2. Saturated spectral quantum efficiency at $V_{op} = -300\,\text{mV}$ and at different V_G values in Y_2O_3 passivated GDs. Inset: Peak responsivity (at 9 μm) and the quantum efficiency at peak responsivity of the UGDs at different V_{op} values.

where σ_{SiO_2} and $\sigma_{Y_2O_3}$ are charge densities of SiO_2/T2SL and Y_2O_3/T2SL interfaces, ε_{SiO_2} and $\varepsilon_{Y_2O_3}$ are dielectric constants of SiO_2 and Y_2O_3, $V_{G,sat}^{SiO_2}$ and $V_{G,sat}^{Y_2O_3}$ are the saturated gate bias of SiO_2 and Y_2O_3 passivated GDs, and d_{SiO_2} and $d_{Y_2O_3}$ are the thicknesses of SiO_2 and Y_2O_3 dielectric layers. Due to Y_2O_3 having a higher dielectric constant, $V_{G,sat}^{Y_2O_3} = -30\,\text{V} \approx \frac{1}{3} V_{G,sat}^{SiO_2}$. Since the $\varepsilon_{SiO_2} = 3.9$ and $\varepsilon_{Y_2O_3}$ is usually reported in the range between 12 and 18 (Refs. 24–27) and both dielectric passivation layers have the same thickness, the $\sigma_{Y_2O_3}$ can be estimated to be 1–1.5 times of σ_{SiO_2}.

The average dark current densities of both SiO_2 and Y_2O_3 passivated GDs at $V_{G,sat}$ are more than one order of magnitude lower than the UPDs and several orders or magnitude lower than the UGDs. The saturated dark current density of Y_2O_3 passivated GDs is slightly better than that of SiO_2 passivated GDs but within the processing tolerance range.

Figure 1(c) shows the correlation between V_G and the dark current density and the differential resistance area product at $V_{op} = -300\,\text{mV}$ ($J_{-300\text{mV}}$ and $RA_{-300\,\text{mV}}$). For $V_G < V_{Gsat} = -30\,\text{V}$, the $J_{-300\text{mV}}$ and $RA_{-300\text{mV}}$ values stay at the level of 2.5×10^{-5} A/cm^2 and $1.3 \times 10^4\ \Omega\,\text{cm}^2$, respectively. According to Ref. 12, for $0\,\text{V} > V_G > -10\,\text{V}$, the type of the mesa sidewall surface is inverted (region I) and the surface depletion width is maximum. For $-10\,\text{V} > V_G > -30\,\text{V}$, the mesa sidewall surface gets into the depletion region (region II). For $V_G < -30$ V, the mesa sidewall surface is at flat band condition or under accumulation (region III). The optical response of the $100 \times 100\ \mu$m UGD array is shown in inset of Figure 2. At $V_{op} = -300\,\text{mV}$, the peak responsivity ($\lambda = 9\ \mu$m) and QE at peak responsivity (noted as $QE_{-300\text{mV}}^{peak}$) of UGD arrays equals 3.7 A/W and 51%, respectively.

The spectral QE curves of $100 \times 100\ \mu$m GD arrays at $V_{op} = -300\,\text{mV}$ and at different V_G values are shown in Figure 2. At $V_G = 0\,\text{V}$, $QE_{-300\text{mV}}^{peak}$ of GDs equals to that of UGDs ($QE_{-300\text{mV}}^{peak} = 51\%$), and it increases with the absolute value of V_G. At $V_G = -15\,\text{V}$, $QE_{-300\text{mV}}^{peak}$ reaches 56%, and at $V_G = -30\,\text{V}$ $QE_{-300\text{mV}}^{peak}$ reaches 57%. The measured quantum efficiency of GDs is determined by the difference between the bulk photocurrent and the recombination rate of photo-generated carriers at the surface.[29] This mesa surface recombination effect is expected to reduce the photocurrent more severely when the mesas are scaled down to the FPA pixel dimension.[30]

Despite the fact that the dark current density undergoes one order of magnitude reduction from $V_G = -15\,\text{V}$ to $V_G = -30\,\text{V}$ (Figure 1(c)), the change of $QE_{-300\text{mV}}^{peak}$ is not obvious for $V_G < -15\,\text{V}$. This difference in behavior between the photocurrent and the dark current might come from the fact that at 77 K, the bulk dark current density is much smaller than the bulk photocurrent density. For $V_G < -15\,\text{V}$, the surface is in the depleted regime(region II), the photocurrent losses due to the surface recombination become negligible compared to the bulk photocurrent, but the surface originated dark current is still very large compared to the bulk dark current.

Temperature dependent measurements of sample C's electrical performance were carried out between 77 K and 150 K. The $RA_{-300\text{mV}}$ and $J_{-300\text{mV}}$ of the UGD and GD array at $V_G = -30\,\text{V}$ at different temperatures are shown in Figure 3. Due to surface leakage suppression, the dark current density of the GDs is lower than that of UGDs at all considered temperatures. The surface leakage does not change with temperature as fast as other bulk dark current mechanisms as can be deduced from the UGD data.[11]

The specific detectivity (D*) of Y_2O_3 passivated UGDs and GDs at $V_G = -30\,\text{V}$ are shown in Figure 4. From 0 to -500 mV, the D* of UGDs decreases by more than one order of magnitude, from 1.7×10^{11} Jones to 3.2×10^9 Jones. In contrast, the D* of the GDs at $V_G = -30\,\text{V}$ keeps increasing from 3.6×10^{11} Jones at 0 mV to 1.4×10^{12} Jones at -300 mV and stays above 10^{12} Jones up to -500 mV. Therefore the GDs can achieve much better electrical and optical characteristics than the UGDs and in a wider operation range.[12]

Figure 5(a) shows the peak detectivity ($\lambda = 9\ \mu$m) of the GDs at $V_G = -30\,\text{V}$ at different V_{op} values from 77 K to 150 K. The level of D* is stable after $V_{op} = -300$mV. The maximum value of peak detectivity ($\lambda = 9\ \mu$m, $V_{OP} = -300\,\text{mV}$) at each temperature and the line of background limited performance (BLIP) detectivity at 9 μm are

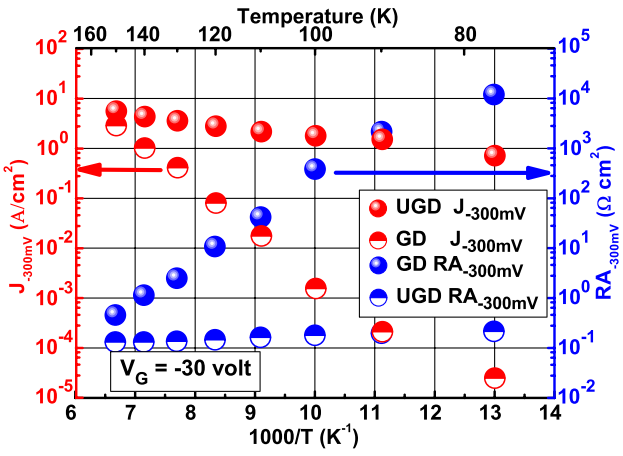

FIG. 3. The evolution of the $J_{-300\text{mV}}$ and $RA_{-300\text{mV}}$ of Y_2O_3 passivated GDs and UGDs at $V_G = -30\,\text{V}$ with temperature.

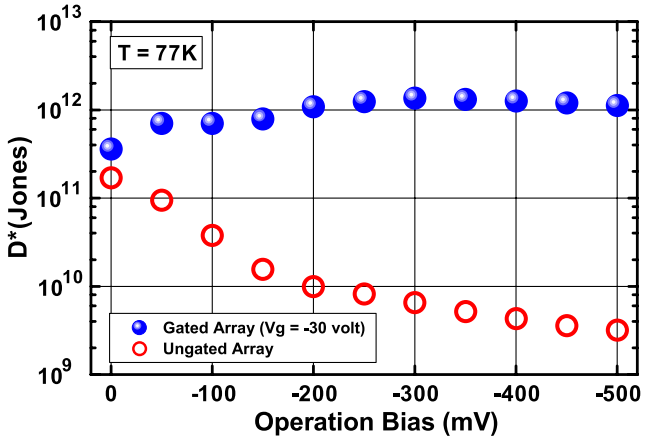

FIG. 4. Specific detectivity of Y_2O_3 passivated UGD array and GD array at $V_G = -30$ V calculated at different V_{op} values.

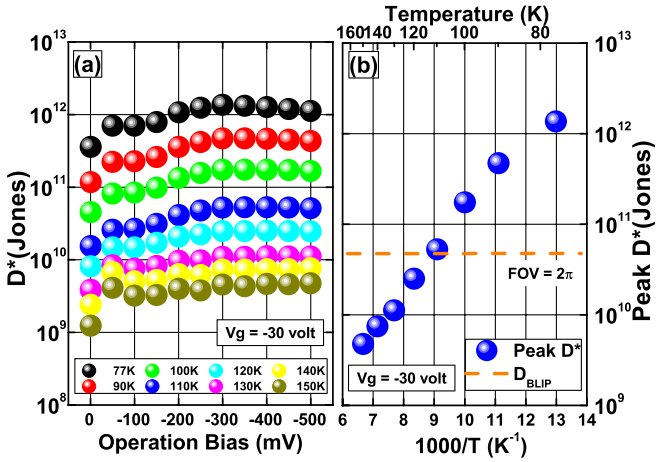

FIG. 5. (a) The evolution of the detectivity of Y_2O_3 passivated gated diode array with temperature at $V_G = -30$ V and different V_{op}. (b) The evolution of the peak detectivity of Y_2O_3 passivated gated diode array with temperature. The peak detectivity crosses the BLIP line at 110 K.

plotted in Figure 5(b). The BLIP temperature is determined as the temperature at which the detectivity of the device is equal to that of an ideal photodiode with 100% QE and a 2π field-of-view (FOV) in a 300 K background. As the temperature increases, the peak detectivity of the GD decreases and intersects with the BLIP detectivity at 110 K.

In summary, we studied the effect of the gating technique on both the electrical and optical characteristics of type-II photodetector array. Passivation with a high-k dielectric, Y_2O_3 decreased saturated gate bias by 3 times compared to the SiO_2 passivation while yielding similar interface charge density. Additional surface treatment is required before or after passivation in order to improve the interface quality. Thanks to the gating technique assisted surface recombination reduction, the quantum efficiency was improved by 12% in $100 \times 100\ \mu$m size detectors. At saturated gate bias and at 77 K, the gated diode array exhibits J_{-300mV} of 2.5×10^{-5} A/cm^2, RA_{-300mV} of $1.3 \times 10^4\ \Omega$ cm^2, a 57% quantum efficiency, and a detectivity of 1.4×10^{12} Jones with a gate bias of -30 V. Moreover, the gated photodetector array showed BLIP temperature of 110 K, demonstrating a strong potential for FPA application.

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